UNIVERSITY OF ENGINEERING AND MANAGEMENT, KOLKATA

In collaboration with

SCHOOL OF VLSI TECHNOLOGY, IIEST SHIBPUR

&

In association with

COMPUTER SOCIETY OF INDIA (CSI) AND THE INSTITITUTION OF ELECTRONICS AND TELECOMMUNICATION ENGINEERS (IETE)

PRESENTS

2024 SUMMER SCHOOL

On

Memory Design & In-Memory Computing

Duration: 29th June-10th July 2024
Days: TBA
Time: 11 am – 1:15 pm & 2 pm-4:15 pm
Course Fees: INR 3000/-+18% GST
Offered by: Department of CST & CSIT in collaboration with School of VLSI Technology, IIEST Shibpur.
Instruction Mode: Online
Open Seats: 30

USP of the Course

"Joining our summer school isn't just about learning; it's about shaping your career in the fast-paced, ever-expanding world of computing technologies. There's no better way to start than with Memory Design & In-Memory Computing, which is poised to drive the data-driven market of the AI era. The demand for memory design engineers in the semiconductor industry is increasing daily and is expected to grow exponentially, especially with the adoption of FinFET nodes. Additionally, the cutting-edge technology of in-memory computing is set to revolutionize analytics and machine learning (you can find more in this article: https://www.linkedin.com/pulse/top-companies-in-memory-computing-market/). Therefore, now is a great time to prepare for industry demands in memory design and stay updated with core concepts of IMC."

Our program isn't like any other - it's designed with one goal in mind: to make you semiconductor industry-ready in the field of digital memory design and IMC technology that can change the dimension of data driven arena like AI/ML or Data Analytics. Here's why our sessions are your best bet for breaking into the world of semiconductor industry as a memory design professional:

1. **Practical Experience:** Unlike many theoretical courses, this program offers students a hands-on experience with core concepts of memory design and in-memory computing at the hardware level. Students will have the opportunity to work directly with industry standard technology nodes, gaining practical skills that are highly sought after in the industry.

2. **Cutting-Edge Technology:** Use of **FinFET** & other lower technology nodes in memory design are the cutting-edge technologies those are transforming memory circuit design. By focusing on the circuit components of memory students will be at the forefront of technological progress, establishing themselves as early adopters and specialists in a fast changing sector. Learners will get to know how is the IMC is making its presence from research arena to industry.

3. **Expert Guideline:** The course will be taught by experts from semiconductor industry, research and academia with extensive experience in digital memory design and in-memory computing. Students will benefit from their expertise, gaining insights and practical knowledge that go beyond what can be found in textbooks or online resources.

4. ****Real-World Application**:** Both the digital memory design & In-Memory Computing (IMC) hold significant promise for Machine Learning (ML**)** and Deep Learning (DL) applications, offering potential benefits in terms of performance, scalability, and energy efficiency.

5. ****Real-time Project based Evaluation****: All the participants will get to work on real-time projects as per the industry standard used cases.

Prerequisite: Basic knowledge in fundamentals of Electronics, MOSFET device physics, digital logic design, computer architecture and elementary programming skills.

Course Summary:

This course covers fundamental and advanced memory technologies in computing. Sessions explore memory hierarchy, SRAM, DRAM, NAND, NOR flash, EDA tools, and memory architecture. Advanced topics include emerging technologies, design verification, lower technology nodes, and in-memory computing (IMC) with practical implementations with final project.

Duration: 2.5 weeks (2 days per week)

Week 1: Introduction to Memory Design

- Session 1 (theory + lab) - Overview of memory hierarchy and types of memory in computing, focus on SRAM, DRAM, NAND flash and NOR flash: characteristics, advantages and applications. Familiarization with EDA tools Cadence Virtuoso, LT-spice (open source), and semiconductor process technologies. **(2 hrs. + 2 hrs.)**
- Session 2 (Interactive theory session): Understanding of basic digital memory design flow followed by the industry: Architecture, circuit design, physical implementation, compiler automation, characterization, timing and model generation. **(1 hr.)**
- Session 3 (theory + lab) - Memory architecture, row/column access, addressing schemes and decoding, sense amplifier and periphery circuits. Setting up of development environment for simulations using LT-spice or Cadence and understanding basic memory operations with 6T-SRAM cell-read/write & stability analysis, Memory performance optimization: timing & speed consideration, low power design & noise immunity. **(1 hr. + 2 hr.)**

Week 2: Advanced Memory Technologies & IMC

- Session 4 (theory) – Emerging Memory Technologies, NVM, 3D stacking and packaging. **(1 hr.)**
- Session 5 (theory + lab) – Design verification and testing of memory. **(1 hr. + 2 hr.)**
- Session 6 (theory + lab) - Overview on lower technology nodes: structure operation and benefits, step-by-step guidance on basic memory cell design and simulation using lower technology node: selection of W/L ratios, supply voltages etc. **(1 hr. + 1 hr.)**
- Session 7 (theory + lab) – Overview on IMC, parallel processing technique in IMC architecture. Implementing a simple IMC-based application prototype. **(1 hr. + 1 hr.)**

Week 3: Final Project and Q&A

- Session 8 (theory)- Final prototype implementation based on given project.
- Session 9 (Q&A and Feedback)- Feedback session and Q&A.

In this 18 hours course, students will explore the principles, applications, and implementation of digital memory design techniques used by semiconductor industries. Participants will be able to learn cutting edge industry standards and new technologies like in-memory computing (IMC) from a hardware perspective. The course covers topics such as memory technologies, hardware design, real-world applications, and future trends. Through a combination of theory sessions and hands-on labs, students will gain practical experience in designing and optimizing memory subsystems systems. By the end of the course, students will be equipped with the skills and insights to understand, design Digital Memory and IMC architectures for various computational challenges.

Eligibility Criteria:

- For IEM Students: Must be currently enrolled as a degree-seeking student at IEM, Kolkata (Newtown Sector) or IEM, Kolkata (Saltlake Sector)
- For Non-IEM Students: - Age Requirement: Applicants must be at least 18 years old by the start of the courses.

Students from B.E./ B.Tech (II year onwards)/ M.Tech/ Ph.D scholars (enrolled) from equivalents branches of ECE/CS/IT/EEE.

For M. Tech Students/ Research Scholars: Registered PhD Scholars and M.Tech students from Recognised Indian Institutes/ Universities.

Working professionals from industry & academicians are also eligible.

- - English Language Proficiency: Must demonstrate proficiency in English as per the specified requirement.

- Application: Students must complete the Summer Sessions application to gain access to enrol in summer courses. Please note that eligibility criteria may be subject to updates or changes, and prospective applicants should verify the latest requirements on the official UEM website.

***Sessions 2, 3 & 6 are sessions from industry experts